A1

width setting delay generator, and a PLL frequency synthesizer having the programmable delay generator inserted between the frequency divider and a phase comparator.--

Please replace the paragraph beginning at page 3, line 3, with the following rewritten paragraph:

A2

--For accomplishing the above object, one aspect of the present invention is a configuration in which a clock is input and an output clock having a phase difference relative to the input clock, the phase obtained by adding or subtracting to or from said phase by a predetermined unit value of a phase differential, on each constant period, is output.--

Please replace the paragraph beginning at page 3, line 10, with the following rewritten paragraph:

--In accordance with another aspect of the present invention, a clock control circuit comprises control means for outputting a control signal for adding or subtracting to or from the phase of an output signal relative to a reference clock, which is an input clock or a clock generated from the input clock, on each clock period of the reference clock, and phase adjustment means fed with the input clock for generating and outputting output clock having a phase corresponding to adding or subtracting a preset unit value of a phase differential to or from a phase with respect to the reference clock, based on the control signal, whereby an output clock of a frequency in a non-integer relation to the frequency of the reference clocks can be output.--

Please replace the paragraph bridging pages 3 and 4, beginning at page 3, line 22, with the following rewritten paragraph:

--Another aspect of the present invention is a clock control circuit comprising a frequency divider for outputting frequency-divided clock obtained on frequency dividing the input clock, a control circuit for generating a control signal for adding or subtracting a unit phase

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difference to or from the input clock with respect to the frequency-divided clock based on the frequency divided clock output from the frequency divider and a phase adjustment circuit fed with the input clock and generating and outputting an output clock having a phase prescribed by the control signal from the control circuit.--

A2

Please replace the paragraph beginning at page 4, line 7, with the following rewritten paragraph:

--Another aspect of the present invention is a clock control circuit comprising a multi-phase clock generating circuit for generating and outputting first to nth clocks having respective different phases (multi-phase clocks) from a phase of the input clock, a selector fed with the first to nth clocks to selectively output one of the clocks, and a control circuit fed with the input clock to generate a control signal sequentially selecting the first to nth clocks to send the generated selection signal to the selector.--

Please replace the paragraph beginning at page 4, line 15, with the following rewritten paragraph:

--Another aspect of the present invention is a clock control circuit comprising an interpolator receiving a frequency divided signal produced by a frequency dividing circuit receiving a clock signal and a signal obtained by shifting the frequency divided signal in a preset number of periods of the clock to produce a signal obtained on division of a timing difference of said two input signals at a preset ratio of internal division; and

a control circuit for varying the value of the ratio of the internal division of the timing difference in said interpolator based on said clock signals.--

Please replace the paragraph bridging pages 4 and 5, beginning at page 4, line 25, with the following rewritten paragraph:

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--Another aspect of the present invention is a clock control circuit comprising a plurality of (N) interpolators for outputting signals obtained on dividing a timing difference of two input signals with respective different values of a preset ratio of internal division; wherein of first to nth clocks with respective different phases, two clocks, that is the Ith and the (I+1)st clocks, where I is an integer from 1 to N, with N+1 being 1, are input to the Ith interpolator.--

Please replace the heading at page 10, line 17, with the following rewritten heading:

--PREFERRED EMBODIMENTS OF THE INVENTION--

Please replace the paragraph bridging pages 10 and 11, beginning at page 10, line 18, with the following rewritten paragraph:

--Preferred embodiments of the present invention are described below. In a preferred embodiment of the present invention, a clock control circuit comprises a control circuit (102 of Fig.1) for outputting a selection control signal for selecting incrementing (adding) or decrementing (subtracting) to or from a phase relative to a reference clock by a predetermined unit value of a phase differential on each reference clock cycle, which is an input clock or a clock generated from an input clock; and a phase adjustment circuit (101 of Fig.1) fed with the input clock and generating an output clock having a phase corresponding to incrementing or decrementing a predetermined unit phase value of a phase differential with respect to the reference clock, based on the control signal, whereby an output clock of a frequency in a non-integer relation with respect to the frequency of the reference clock can be output.--

Please replace the paragraph beginning at page 11, line 7, with the following rewritten paragraph:

--In another preferred embodiment of the present invention, a clock comprises a frequency divider (103 of Fig.3) for outputting frequency-divided clocks obtained by frequency

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